PATENT

METHOD AND APPARATUS OF ALLOCATING MINIMUM AND MAXIMUM BANDWIDTHS ON A BUS-BASED COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to a method and apparatus of allocating bandwidth on a bus-based communication system and, more particularly, to a method and apparatus of allocating minimum and maximum bandwidths on a bus-based communication system.

2. Description of the Related Art.

A bus-based communication system is a system that allows a number of communication circuits to exchange signals with each other over a group of shared electrical pathways. For example, the communication circuits on service cards, such as xDSL and other line cards, can be connected to, and communicate over, a bus.

FIG. 1 shows a block diagram that illustrates a conventional bus-based communications system 100. As shown in FIG. 1, system 100 includes a cell bus 110 that has a first bus BUS-A and a pair of first-bus control lines SEL-A0 and SEL-A1. In addition, cell bus 110 also includes a second bus BUS-B, and a pair of second-bus control lines SEL-B0 and SEL-B1. First bus BUS-A utilizes a first group of electrical pathways, such as eight electrical pathways that represent eight bits, while second bus BUS-B utilizes a second group of electrical pathways, such as eight electrical pathways that represent eight bits.

As further shown in the FIG. 1 example, system 100 also includes a number of service cards 112 that are connected to cell bus 110. Each

service card 112 is also connected to a number of network devices 114 to receive a number of streams of data cells DS. The data cells DS can have different priority levels such that a data cell DS from one network device 114 is preferred over the data cell DS from another network device 114.

Each service card 112 includes a communication circuit 116 that has a transmit circuit 120 that transmits data cells onto cell bus 110, and a receive circuit 122 that receives data cells from cell bus 110. Communication circuit 116 also includes a logic block 124 that processes the data cells DS.

In operation, when a number of communication circuits 116 are connected to cell bus 110, one of the communication circuits 116 assumes the role of bus master, while the remaining communication circuits 116 assume the roles of bus slaves and communicate over the bus as allowed by the bus master.

The bus master controls the timing of the bus along with access to the bus. For example, the bus master can define transmission periods on bus BUS-A and bus BUS-B, and determine the communication circuit 116 that has permission to use each of the transmission periods on the buses.

FIG. 2 shows a state diagram that illustrates a prior art state machine 200 operating as a bus master. State machine 200 is executed by the logic block 124 of the communication circuit 116 that is the bus master. As shown in FIG. 2, state machine 200 begins at state 210 by determining whether any requests to use bus BUS-B were received during a first request period.

Requests to use bus BUS-B are received during request periods where each communication circuit 116 that wishes to transmit a data cell over bus 110 outputs a request. The requests are output over select lines SEL-A0, SEL-A1, SEL-B0, and SEL-B1 to the bus master.

Each request period can be, for example, 12 clock cycles long to support 24 communication circuits 116.

For example, a 1st communication circuit can request bus BUS-B during a first-request clock cycle of a request period on select line SEL-A0 and SEL-A1, while a 13th communication circuit can request bus BUS-B during the first-request clock cycle on select lines SEL-B0 and SEL-B1. In addition, a 2nd communication circuit can request bus BUS-B during a second-request clock cycle on select line SEL-A0 and SEL-A1, while a 14th communication circuit can request bus BUS-B during the second-request clock cycle on select lines SEL-B0 and SEL-B1. Thus, in this example, after 12 clock cycles, each of 24 communications circuits has had a one clock cycle opportunity to request control of bus BUS-B over select lines SEL-A0, SEL-A1, SEL-B0, and SEL-B1.

Each communication circuit 116 outputs a logic value onto the select lines SEL during its assigned clock cycle to indicate whether a request is being made and, if so, the priority level of the request. For example, a logic value of 0-0 can represent a high priority level, while a logic value of 0-1 can represent a medium priority level. In addition, a logic value of 1-0 can represent a low priority level, while a logic value of 1-1 can represent no request.

When requests are received during the first request period, state machine 200 moves to state 212 to define a group of requesting circuits that include the communication circuits 116 that submitted a bus control request during the first request period. For example, state machine 200 can define a group that includes only the communication circuits 116 that requested control of bus BUS-B during the first request period.

Following this, state machine 200 moves to state 214 to grant access to one of the group of requesting communication circuits to transmit in the next transmission period on bus BUS-B. Access is granted by outputting a grant to the requesting communication circuit

116 over the control lines SEL-B0 and SEL-B1. States 212 and 214 can be, for example, eight clock periods long. In addition, an error correction code can be transmitted at the same time on the select lines SEL-A0 and SEL-A1 that are not carrying the grant. Once the grant has been output, state machine 200 moves to state 216 to wait for a predefined period of time. The total time required to complete states 210-216 can be, for example, 26 clock cycles.

After the predefined time has expired, state machine 200 moves to state 218 to determine whether any requests to use bus BUS-A were received during a second request period. In the present example, one clock cycle before state machine 200 moves to state 218, the communication circuit 116 that received control over bus BUS-B, begins transmitting a data cell on bus BUS-B.

As with bus BUS-B, requests to use bus BUS-A are also received during a request period where each communication circuit 116 that wishes to transmit a data cell over bus 110 can output a request. The requests are again output over select lines SEL-A0, SEL-A1, SEL-B0, and SEL-B1 to the bus master, and the request period can also be 12 clock cycles long to support 24 communication circuits 116.

For example, a 1st communication circuit can request bus BUS-A during a first-request clock cycle of a next request period on select lines SEL-B0 and SEL-B1, while a 13th communication circuit can request bus BUS-A during the first-request clock cycle on select lines SEL-A0 and SEL-A1. In addition, a 2nd communication circuit can request bus BUS-A during the second-request clock cycle on select lines SEL-B0 and SEL-B1, while a 14th communication circuit can request bus BUS-A during the second-request clock cycle on select lines SEL-A0 and SEL-A1. Thus, in this example, 12 clock cycles after the request period for bus BUS-A began, each of 24 communications circuits has had a one clock

cycle opportunity to request control of bus BUS-A over select lines SEL-A0, SEL-A1, SEL-B0, and SEL-B1.

When requests for bus BUS-A are received during the second request period, state machine 200 moves to state 220 to define a group of requesting circuits that include the communication circuits 116 that submitted a bus control request during the second request period. For example, state machine 200 can define a group that includes only the communication circuits 116 that requested control of bus BUS-A during the second request period.

Following this, state machine 200 moves to state 222 to grant access to one of the group of requesting communication circuits to transmit a data cell in the next transmission period on bus BUS-A. As above, access is granted by outputting a grant to the requesting communication circuit 116 over the control lines SEL-A0 and SEL-A1. States 220 and 222 can be, for example, eight clock periods long. In addition, an error correction code can be transmitted at the same time on the select lines SEL-B0 and SEL-B1 that are not carrying the grant.

Once the grant has been output, state machine 200 moves to state 224 to wait for a predefined period of time. The total time required to complete states 218-224 can be, for example, 26 clock cycles. After the predefined time has expired, state machine 200 returns to state 210 to repeat the process. In addition, if no requests are received during the first request period, state machine 200 waits until the end of the 26 clock cycle, and then moves from state 210 to state 218. Similarly, if no requests are received during the second request period, state machine 200 waits until the end of the 26 clock cycle, and then moves from state 218 to state 210.

Thus, state machine 200 moves through states 210-216, which define a first arbitration period, to determine and grant permission to transmit a data cell during the next transmission period on bus BUS-B,

and then through states 218-224, which define a second arbitration period, to determine and grant permission to transmit a data cell during the next transmission period on bus BUS-A. As a result, state machine 200 provides an alternating series of arbitration periods where control over bus BUS-B is determined, and then control over bus BUS-A is determined.

FIG. 3 shows a graphical representation that further illustrates prior art state machine 200. As shown in FIG. 3, state machine 200 defines an alternating series of BUS-B and BUS-A arbitration periods 310 and 312, respectively, on control lines SEL-A0, SEL-A1, SEL-B0, and SEL-B1. The BUS-B arbitration period 310 can be implemented with, for example, states 210-216, while the BUS-A arbitration period 312 can be implemented with, for example, states 218-224.

In the FIG. 3 example, following a BUS-B arbitration period 310, the communication circuit 116 that received the grant begins transmitting a data cell on bus BUS-B one clock cycle before the next BUS-A arbitration period 312, and continues transmitting the data cell for a transmit period. The transmit period can be, for example, 52 clock cycles long.

Similarly, following a BUS-A arbitration period 312, the communication circuit 116 that received the grant begins transmitting a data cell on bus BUS-A one clock cycle before the next BUS-B arbitration period 310, and continues transmitting the data cell for the transmit period.

Thus, as shown in FIG. 3, when a communication circuit 116 receives control over one of the two buses, such as BUS-A, the circuit 116 transmits the data cell over the bus during the next two arbitration periods. By utilizing two 26-cycle arbitration periods and one 52-cycle transmit period, a single 52 byte ATM cell can be transmitted.

FIG. 4 shows a flow chart that illustrates a prior art method 400 of granting access to a bus to one of a number of requesting communication circuits. In the present case, each of the requesting communication circuits submitted a bus control request to the bus master during the same request period.

As shown in FIG. 4, method 400, which can be used to implement steps 214 and 222, begins at step 410 by identifying the requesting communication circuits 116 that wish to transmit a high priority data cell. Priority can be divided into different levels, such as high, medium, and low, and assigned to different data cells DS so that a data cell DS with a high priority is preferred over a data cell DS with a medium or low priority, while a data cell DS with a medium priority is preferred over a data cell DS with a low priority.

If no communication circuits with a high priority data cell requested control, method 400 moves to step 412 to identify the requesting communication circuits 116 that wish to transmit a medium priority data cell. If no communication circuits with a medium priority data cell requested control, method 400 moves to step 414 to identify the requesting communication circuits that wish to transmit a low priority data cell.

Once the requesting communication circuits within a priority level have been identified, method 400 moves from either step 410, step 412, or step 414 to step 416 to determine which of the communication circuits within the priority level will receive the grant (permission to transmit during the next transmission period).

When several requesting communication circuits 116 have the same priority level, the requesting communication circuit 116 to receive the grant can be defined by an arbitration, such as a declining round robin. In a declining round robin, the requesting communication circuits 116 circulate within a hierarchical ranking.

The requesting communication circuit at the top of the ranking is assigned the grant and, after receiving the grant, moves to the bottom of the ranking. The ranking of a communication circuit 116 increases each time the circuit is denied a grant, i.e., control of the bus.

One drawback with method 400 is that if the requesting communication circuits 116 with high priority data streams are over subscribed, method 400 can always or nearly always move from step 410 to step 416. As a result, the higher priority data cells DS can consume all of the available bandwidth, thereby preventing the lower priority data cells DS from being transmitted onto the bus. Thus, there is a need for a method and apparatus that grants access to a bus that insures that lower priority data streams are able to transmit information across the bus.

SUMMARY OF THE INVENTION

The present invention provides a method and an apparatus that grant access to a bus to one of a plurality of requesting communication circuits that each submitted a bus control request during a request period of an arbitration period. The method includes the step of determining a stored identity associated with the arbitration period, and determining whether any requesting communication circuit has an identity that matches the stored identity. The stored identity identifies a communication circuit.

The present invention also includes a communication circuit that includes a transmit circuit that transmits information onto a cell bus, and a receive circuit that receives information from the cell bus. The communication circuit also includes a memory that stores priority information regarding a plurality of arbitration periods. The priority

information for each arbitration period includes a stored identity that identifies a communication circuit.

The communication circuit additionally includes a logic circuit that is connected to the transmit circuit, the receive circuit, and the memory, and determines whether any communication circuits requested control of a bus during an arbitration period. The logic circuit reads a stored identity associated with the arbitration period, and determines whether any requesting communication circuit has an identity that matches the stored identity. The stored identity identifies a communication circuit.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings that set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a conventional bus-based communications system 100.

FIG. 2 is a state diagram illustrating a prior art state machine 200 operating as a bus master.

FIG. 3 is a graphical representation further illustrating prior art state machine 200.

FIG. 4 is a flow chart illustrating a prior art method 400 of granting access to a bus to one of a number of requesting communication circuits.

FIG. 5 is a block diagram illustrating an example of a bus-based communications system 500 in accordance with the present invention.

FIG. 6 is a state diagram illustrating an example of a state machine 600 that grants access to a bus to one of a number of

requesting communication circuits in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 5 shows a block diagram that illustrates an example of a bus-based communications system 500 in accordance with the present invention. System 500 is similar to system 100 and, therefore, utilizes the same reference numerals to designate the structures which are common to both systems.

As shown in FIG. 5, system 500 differs from system 100 in that system 500 includes a memory 510 that stores grant information that is associated with each of a number of arbitration periods. The grant information, which can be organized as a Priority Table, can be stored in a number of memory devices, including registers and non-volatile memory cells.

An example of a Priority Table is shown below. The Priory Table includes a number of rows of data where each row corresponds with an arbitration period. (As described above, an arbitration period can be a 26 clock cycle period where requests are received during a request period and a grant is output.) Thus, a Priority Table that is 512 rows long represents 512 consecutive arbitration periods.

Arbitration Period	Valid Status	Stored Priority	Stored Identity
1	X	XX	XXXXX
2	X	XX	XXXXX
3	X	XX	XXXXX
. . .	...	...	...
512	X	XX	XXXXX

Priority Table

In addition, each row includes a valid status, a stored identity, and a stored priority. The valid status indicates whether the row of data associated with the arbitration period is valid. The stored identity identifies a communication circuit 116, while the stored priority indicates a priority level of a data cell to be transmitted by the communication circuit.

For example, each row of data can include five bits [bits 4:0] of stored identity that identify a communication circuit 116, two bits [bits 6:5] of stored priority that identify one of four priority levels, and one bit [bit 7] of valid status that indicates whether the data in the row associated with the arbitration period is valid.

The four priority levels include a high priority level represented by, for example, a 0-0, and a medium priority level represented by, for example, a 0-1. In addition, the four priority levels also include a low priority level represented by, for example, a 1-0, and an all priority level represented by, for example, a 1-1.

As further shown in FIG. 5, system 500 also differs from system 100 in that system 500 includes a logic circuit 512 and a high priority register 514 that indicates whether the high priority data received by a

communication circuit 116 is arbitration, such as round robin, enabled. System 500 also includes a medium priority register 516 that indicates whether the medium priority data received by the communication circuit 116 is arbitration enabled, and a low priority register 518 that indicates whether the low priority data received by the communication circuit 116 is arbitration enabled.

System 500 can operate the same as state machine 200 in determining a group of requesting circuits, as illustrated in states 210, 212, 218, and 220 shown in FIG. 2. FIG. 6 shows a state diagram that illustrates an example of a state machine 600 that grants access to a bus to one of a number of requesting communication circuits in accordance with the present invention. State machine 600 can be used to implement states 214 and 222 shown in FIG. 2.

In the present example, the logic circuit 512 of the bus master has determined the requesting communication circuits that submitted a bus control request to the bus master during the same request period of an arbitration period, such as in states 210, 212, 218, and 220. Method 600 can be executed by the memory 510 and logic circuit 512 of the communication circuit 116 that is the bus master in system 500.

A shown in FIG. 6, state machine 600 begins at state 610 by determining if the grant information that is associated with the arbitration period, such as the information stored in the row of the Priority Table that corresponds with the arbitration period, is valid, such as by checking the valid bit in the row of the Priority Table. The row of the Priority Table is selected to correspond with the arbitration period. For example, the first row of the table can correspond with the first arbitration period, and the 513^{th} arbitration period when a 512 row Priority Table is used.

When the valid bit indicates that the information is valid, state machine 600 moves to state 612 to determine the stored identity that is

associated with the arbitration period, such as by checking the identity bits in the row of the Priority Table that corresponds with the arbitration period. In addition, state machine 600 also determines in state 612 whether any requesting communication circuit has an identity that matches the stored identity.

When a requesting communication circuit has an identity that matches the stored identity, state machine 600 moves to state 614 to identify the requesting communication circuit as a matching communication circuit, and determine the stored priority that is associated with the arbitration period, such as by checking the priority bits in the row of the Priority Table that corresponds with the arbitration period. In addition, state machine 600 also determines in state 614 whether the priority of the data cell of the matching communication circuit matches the stored priority read from the row of the Priority Table.

When the priority of the data cell of the matching communication circuit matches the stored priority, state machine 600 moves to state 616 to output a grant to the matching communication circuit. The grant gives the matching communication circuit 116 permission to transmit during the next transmission period on a bus.

In state 610 when the grant information is invalid, in state 612 when a requesting communication circuit does not have an identity that matches the stored identity, and in state 614 when the matching communication circuit does not have a priority that matches the stored priority, state machine 600 moves to state 620 to determine whether any of the requesting communication circuits 116 wishes to transmit a high priority data cell. In addition, state machine 600 also determines in state 620 which of the high priority communications circuits are also arbitration enabled, such as by checking the high priority registers 514 on the communication circuits 116.

When an arbitration-enabled requesting communication circuit has a high priority data cell, state machine 600 moves to state 622 to determine which of the arbitration enabled communication circuits within the priority level will receive the grant (permission to transmit during the next transmission period).

When several requesting communication circuits 116 have the same priority level, the requesting communication circuit 116 to receive the grant can be defined by an arbitration, such as a declining round robin. As noted above, in a declining round robin, the requesting communication circuits 116 circulate within a hierarchical ranking.

After state machine 600 has selected a communication circuit from the arbitration, state machine 600 moves to state 616 to send a grant to the selected communication circuit. The grant gives the selected communication circuit 116 permission to transmit during the next transmission period on the bus.

If no communication circuits with a high priority data cell requested control, state machine 600 moves to state 624 to identify the requesting communication circuits 116 that wish to transmit a medium priority data cell. In addition, state machine 600 also determines in state 624 which of the medium priority communications circuits are also arbitration enabled, such as by checking the medium priority registers 516 on the communication circuits 116.

When an arbitration-enabled requesting communication circuit has a medium priority data cell, state machine 600 moves to state 622 to determine which of the communication circuits within the priority level will receive the grant (permission to transmit during the next transmission period). As above, the requesting communication circuit 116 to receive the grant can be defined by an arbitration, such as a declining round robin.

If no communication circuits with a medium priority data cell requested control, state machine 600 moves to state 626 to identify the requesting communication circuits that wish to transmit a low priority data cell. In addition, state machine 600 also determines in state 626 which of the low priority communications circuits are also arbitration enabled, such as by checking the low priority registers 518 on the communication circuits 116.

When an arbitration-enabled requesting communication circuit has a low priority data cell, state machine 600 moves to state 622 to determine which of the communication circuits within the priority level will receive the grant (permission to transmit during the next transmission period). As above, the requesting communication circuit 116 to receive the grant can be defined by an arbitration, such as a declining round robin. (State machine 600 can alternately be implemented in software.)

One of the advantages of the present invention is that the present invention insures that communication circuits with low priority data streams receive a minimum level of service. For example, to insure that a communication circuit 116 with a low priority data cell is able to transmit at least once every 512 arbitration cycles, where the Priority Table has 512 rows, the communication circuit 116 can be listed in one row with a low priority level type.

If a low priority data cell of the communication circuit 116 is to receive only one grant every 512 arbitration periods, then the low priority register 518 on the communication circuit 116 is set to prevent arbitration. If the low priority data cell of the communication circuit 116 is to receive at least one grant, but maybe more than one grant, every 512 arbitration periods, then the low priority register 516 is set to allow arbitration.

Another advantage is that the present invention can insure that communication circuits with a high priority data stream receive a known level of service. For example, to insure that a communication circuit 116 with a high priority data stream is able to transmit 150 times every 512 arbitration cycles, where the Priority Table has 512 rows, the communication circuit 116 can be listed in 150 rows with a high priority level type, and arbitration register 514 set to prevent arbitration.

Thus, not only does the present invention limit the bandwidth that a high priority user can have, thereby allowing low priority users to transmit on the bus, the present invention also guarantees the high priority user a predetermined bandwidth that is free from competition from other high priority users. Other levels of service can also be provided by varying the priority level and the enable status.

It should be understood that the above descriptions are examples of the present invention, and that various alternatives of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.